Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 2, 7, 8, 18, 21-25, 28, and 29 have been amended. Claims 3, 9, 20, and 27 have been cancelled. No claims have been added. Claim 4 was previously cancelled. Claims 10-17 were previously withdrawn. Therefore, claims 1, 2, 5-8, 18, 19, 21-26, 28, and 29 are presented for examination.

Specification

The specification has been amended to appear in better form for allowance. Specifically, the title has been amended in line with the Examiner's suggestion. In addition, the abstract has been amended to sufficiently describe the disclosure. Applicants respectfully requests that the objections to the specification be withdrawn.

In addition, applicant has amended paragraph [0047] of the specification to recapture erroneously deleted material. Applicant did have intent to claim the recaptured material.

Drawings

The drawings and the specification have been amended to place the drawings in better form for allowance. Specifically, the Examiner queries that "it is not clear what is mean by LDTI/LDFI into debug instruction. How is an instruction into another instruction? What does this mean?" (Final Office Action mailed 10/17/2007 at pg. 3.) Figure 8B has been corrected and a replacement drawing sheet submitted in its place. Specifically, Figure 8B now states "LDTI Into Debug Instruction *Register*" and "LDFI

Into Debug Instruction *Register*" (emphasis added). This amendment should clarify the meaning of the particular processing blocks referenced. Applicant respectfully requests that the objections to the drawings be withdrawn.

In addition, Figure 8A is being correct and replaced with a submitted replacement drawing sheet. Specifically, minor typographical errors are being correct in reference blocks 840, 850, and 890.

Claim Objections

Claim 24 stands objected to because of the following informalities: The Examiner states that "[i]f applicant wishes to use "adding" instead of --attaching-- in line 2, then please replace "attached" with --added-- in line 6 for consistency and increased clarity." (Final Office Action mailed 10/19/2007 at pg. 3.) However, applicant submits that claim 24 as it stands is in line with the Examiner's suggestion. The claim as previously amended replaced both of the "attaching" terms in lines 2 and 6, with the "adding" term. In addition, the claim has now been further amended to replace the second "adding" term language with the term "manipulating." As such, Applicant submits that the present claim objection is therefore moot. Applicant respectfully requests that the objection to the claim be withdrawn.

35 U.S.C. § 112 Rejection

Claims 1, 18, and 24 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Specifically, the Examiner states that "it is not known what is meant by adding at least three fields to a control status register."

(Final Office Action at pg. 4.) Claims 1, 18, and 24 have been amended to remove the "adding" claim language that is the basis of this rejection. These claims now refer to "manipulating" the three fields of the control status register. As such, it is now clear that these fields could be assigned and manipulated at run-time for the benefit of the debugging process of embodiments of the present application. In addition, the uncertainty and confusion resulting from the "adding" and/or "attaching" language is now moot. As a result, applicant submits that the §112 rejection has been overcome and respectfully requests that the rejection be withdrawn.

Claims 2-3, 5-9, 19-23, and 25-29 stand rejected under 35 U.S.C. § 112, first paragraph, for being non-enabling, because they are dependent, either directly or indirectly, on a non-enabling claim. For the reasons above, these claims have overcome the §112 rejection and applicant respectfully requests that the rejection be withdrawn.

35 U.S.C. §103(a) Rejection

Claims 1-3, 5-9, and 18-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Glew et al. (U.S. Patent No. 5,694,589) in view of Deng et al. (U.S. Patent No. 6,951,416). Applicant submits that the present claims are patentable over Glew in view of Deng.

Glew discloses code breakpoint detection logic for a superscalar microprocessor. (Glew at Abstract.) Deng discloses debugger circuitry that is implemented on the microcontroller itself and that may break application program execution upon detection of a specified condition, display internal register values to the user, and continue the application program execution. (Deng at col. 2, ll. 37-41.)

Claim 1, as amended, recites:

An apparatus comprising:
a memory;
a plurality of processors coupled to the memory; and
a controller coupled to the memory and the plurality of processors, the controller to execute a debug process that:
attaches at least one breakpoint bit field directly to one or more instructions of the plurality of processor, the breakpoint bit field to enable a user of the apparatus to set a breakpoint based on an address of the particular instruction without having to perform an address comparison;
manipulates at least three debug register bit fields of at least one processor control status register, the at least three register bit fields comprise a run field, a single step field, and a debug enable field; and
accesses an internal status of one or more of the plurality of processors by utilizing at least one of a Load to Instruction RAM instruction (LDTI) and a Load from Instruction RAM (LDFI) instruction.

Applicant submits that Glew does not disclose or suggest a debug process that attaches at least one breakpoint bit field directly to one or more instructions of the plurality of processor, the breakpoint bit field to enable a user of the apparatus to set a breakpoint based on an address of the particular instruction without having to perform an address comparison, as recited in claim 1. Applicant can specifically find no disclosure in Glew of the feature of the breakpoint bit field that enables a user to set a breakpoint based on an address of the particular instruction without having to perform an address comparison. In fact, Glew itself states that the "breakpoint logic 200 will determine if the next fetch IP corresponds to one of the breakpoint addressed stored in the debug address registers of the microprocessor." (Glew at col. 6, ll. 28-31.) This seems to refer to an address comparison process, which is specifically ruled out in the cited claim language of claim 1. As such, Glew cannot disclose or suggest this feature of claim 1.

Furthermore, applicant submits that Glew does not disclose or suggest a debug process that accesses an internal status of one or more of the plurality of processors by utilizing at least one of a Load to Instruction RAM instruction (LDTI) and a Load from Instruction RAM (LDFI) instruction, as recited in claim 1. Applicant can find no disclosure or suggestion of such a feature anywhere in Glew. As such, Glew does not disclose or suggest the cited feature of claim 1.

In addition, applicant further submits that Deng also does not disclose or suggest a debug process that attaches at least one breakpoint bit field directly to one or more instructions of the plurality of processor, the breakpoint bit field to enable a user of the apparatus to set a breakpoint based on an address of the particular instruction without having to perform an address comparison and accesses an internal status of one or more of the plurality of processors by utilizing at least one of a Load to Instruction RAM instruction (LDTI) and a Load from Instruction RAM (LDFI) instruction, as recited in claim 1. The Examiner does not rely on Deng to teach such features and applicant can find no disclosure or suggestion of these features anywhere in Deng. As such, Deng does not disclose or suggest the cited features of claim 1.

In conclusion, neither Glew nor Deng, individually or in combination, disclose or suggest the above-cited features of claim 1. As a result, claim 1, as well as its dependent claims is patentable over Glew in view of Deng.

Independent claims 18 and 24 also recite the above-cited features of claim 1. As a result, claims 18 and 24, as well as their respective dependent claims, are also patentable over Glew in view of Deng.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

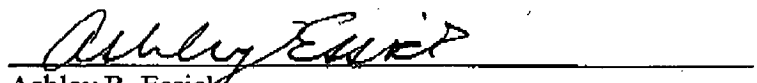
Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: February 14, 2008



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